



# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## General Description

The MAX3394E/MAX3395E/MAX3396E bidirectional level translators provide level shifting required for data transfer in a multivoltage system. Internal slew-rate enhancement circuitry features 10mA current-sink and 15mA current-source drivers to isolate capacitive loads from lower current drivers. In open-drain systems, slew-rate enhancement enables fast data rates with larger pullup resistors and increased bus load capacitance. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic-high levels for the device. A logic-low signal on one I/O side of the device appears as a logic-low signal on the opposite I/O side, and vice-versa. Each I/O line is pulled up to  $V_{CC}$  or  $V_L$  by an internal pullup resistor, allowing the devices to be driven by either push-pull or open-drain drivers.

The MAX3394E/MAX3395E/MAX3396E feature a tri-state output mode, thermal-shutdown protection, and ±15kV Human Body Model (HBM) ESD protection on the  $V_{CC}$  side for greater protection in applications that route signals externally.

The MAX3394E/MAX3395E/MAX3396E accept  $V_{CC}$  voltages from +1.65V to +5.5V, and  $V_L$  voltages from +1.2V to  $V_{CC}$ , making them ideal for data transfer between low voltage ASIC/PLDs and higher voltage systems. The MAX3394E/MAX3395E/MAX3396E operate at a guaranteed data rate of 6Mbps with push-pull drivers and 1Mbps with open-drain drivers.

The MAX3394E is a dual-level translator available in 9-bump UCSP™ and 8-pin 3mm x 3mm TDFN packages. The MAX3395E is a quad-level translator available in 12-bump UCSP, and 12-pin 4mm x 4mm TQFN packages. The MAX3396E is an octal-level translator available in 20-bump UCSP and 20-pin 5mm x 5mm TQFN packages. The MAX3394E/MAX3395E/MAX3396E operate over the extended -40°C to +85°C temperature range.

## Applications

Multivoltage Bidirectional Level Translation  
 SPI™, MICROWIRE™, and I<sup>2</sup>C Level Translation  
 Open-Drain Rise-Time Speed-Up  
 High-Speed Bus Fan-Out Expansion  
 Cell Phones  
 Telecom, Networking, Servers, RAID/SAN

## Features

- ◆ ±15kV ESD Protection on I/O  $V_{CC}$  Lines
- ◆ Bidirectional Level Translation Without Direction Pin
- ◆ I/O  $V_L$  and I/O  $V_{CC}$  10mA Sink-/15mA Source-Current Capability
- ◆ Slew-Rate Enhancement Circuitry Supports Larger Capacitive Loads or Larger External Pullup Resistors
- ◆ 6Mbps Push-Pull/1Mbps Open-Drain Guaranteed Data Rate
- ◆ Wide Supply-Voltage Range: Operation Down to +1.2V on  $V_L$  and +1.65V on  $V_{CC}$
- ◆ Low Supply Current in Tri-State Output Mode (3µA typ)
- ◆ Low Quiescent Current
- ◆ Thermal-Shutdown Protection
- ◆ UCSP, TDFN, and TQFN Packages

## Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX3394EETA+T	8 TDFN-EP**	T833-1
MAX3394EEBL+T	9 UCSP	B9-5
MAX3395EETC+	12 TQFN-EP**	T1244-4
MAX3395EEBC+T	12 UCSP	B12-1
MAX3396EEBP+T*	20 UCSP	B20-1
MAX3396EETP+	20 TQFN-EP**	T2055-4

**Note:** All devices specified over the -40°C to +85°C operating range.

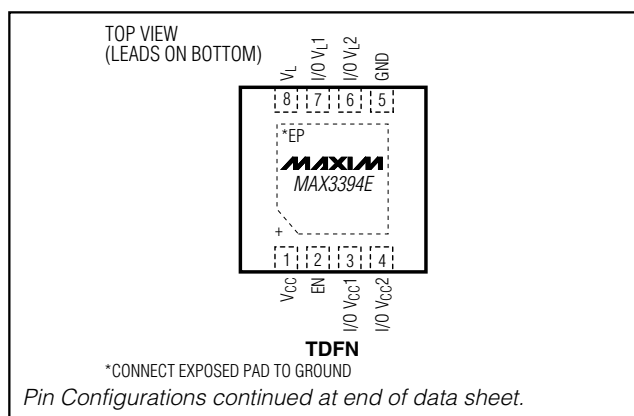
+Denotes lead-free package.

\*Future product—contact factory for availability.

\*\*EP = Exposed paddle.

Selector Guide appears at end of data sheet.

## Pin Configurations



MAX3394E/MAX3395E/MAX3396E

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## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V <sub>CC</sub> .....	-0.3V to +6V
V <sub>L</sub> .....	-0.3V to +6V
I/O V <sub>CC_</sub> .....	-0.3V to V <sub>CC</sub> + 0.3V
I/O V <sub>L_</sub> .....	-0.3V to V <sub>L</sub> + 0.3V
EN .....	-0.3V to +6V
Short-Circuit Duration I/O V <sub>L_</sub> , I/O V <sub>CC_</sub> to GND .....	Continuous
Maximum Continuous Current .....	±50mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
8-Pin TDFN (derate 18.2mW/°C above +70°C) .....	1455mW
9-Bump UCSP (derate 4.7mW/°C above +70°C) .....	379mW

12-Pin TQFN (derate 16.9mW/°C above +70°C) .....	1349mW
12-Bump UCSP (derate 6.5mW/°C above +70°C) .....	519mW
20-Pin TQFN (derate 20.8mW/°C above +70°C) .....	1667mW
20-Bump UCSP (derate 10.0mW/°C above +70°C) .....	800mW
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+150°C
Bump Temperature (soldering) .....	+235°C
Lead Temperature (soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +1.65V to +5.5V, V<sub>L</sub> = +1.2V to V<sub>CC</sub>; C<sub>IOVL</sub> ≤ 15pF, C<sub>IOVCC</sub> ≤ 15pF; T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
V <sub>L</sub> Supply Range	V <sub>L</sub>		1.2		V <sub>CC</sub>	V
V <sub>CC</sub> Supply Range	V <sub>CC</sub>		1.65		5.50	V
Supply Current from V <sub>CC</sub>	I <sub>CC</sub>	I/O lines internally pulled up	MAX3394E		150	μA
			MAX3395E		300	
			MAX3396E		600	
Supply Current from V <sub>L</sub>	I <sub>L</sub>	I/O lines internally pulled up	MAX3394E		30	μA
			MAX3395E		30	
			MAX3396E		30	
V <sub>CC</sub> Tri-State Supply Current	I <sub>CC-3</sub>	EN = GND, T <sub>A</sub> = +25°C		3	6	μA
V <sub>L</sub> Tri-State Supply Current	I <sub>L-3</sub>	EN = GND, T <sub>A</sub> = +25°C		0.7	2	μA
<b>LOGIC I/O</b>						
I/O V <sub>L_</sub> Input-Voltage High Threshold	V <sub>IHL</sub>				0.7 x V <sub>L</sub>	V
I/O V <sub>L_</sub> Input-Voltage Low Threshold	V <sub>ILL</sub>		0.3 x V <sub>L</sub>			V
I/O V <sub>L_</sub> Internal Pullup DC Resistance	R <sub>L</sub>	EN = V <sub>CC</sub> or V <sub>L</sub>	5	10	20	kΩ
I/O V <sub>L_</sub> Source Current During Low-to-High Transition	I <sub>IHL</sub>	V <sub>L</sub> = +1.2V		15		mA
I/O V <sub>L_</sub> Sink Current During High-to-Low Transition	I <sub>ILL</sub>	V <sub>CC</sub> = +1.65V		10		mA

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MAX3394E/MAX3395E/MAX3396E

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +1.65V to +5.5V, V<sub>L</sub> = +1.2V to V<sub>CC</sub>; C<sub>IOVL</sub> ≤ 15pF, C<sub>IOVCC</sub> ≤ 15pF; T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V <sub>L</sub> Low-to-High Transition Threshold	V <sub>L-TH</sub>	V <sub>CC</sub> = +3.3V, V <sub>L</sub> = +1.8V	0.3 x V <sub>L</sub>	0.5 x V <sub>L</sub>		V
I/O V <sub>L</sub> Output-Voltage Low	V <sub>OLL</sub>	I/O V <sub>L</sub> sink current = 4mA, V <sub>IOVCC</sub> = 0V			0.25	V
		I/O V <sub>L</sub> sink current = 8mA, V <sub>IOVCC</sub> ≤ or 0.2 x V <sub>L</sub>			V <sub>ILC</sub> + 0.4V	
I/O V <sub>L</sub> Tri-State Output Leakage Current		EN = GND, T <sub>A</sub> = +25°C	-1		+1	μA
I/O V <sub>CC</sub> Input-Voltage High Threshold	V <sub>IHC</sub>	(Note 2)			0.7 x V <sub>CC</sub>	V
I/O V <sub>CC</sub> Input-Voltage Low Threshold	V <sub>ILC</sub>	(Note 2)	0.3 x V <sub>CC</sub>			V
I/O V <sub>CC</sub> Internal Pullup DC Resistance	R <sub>CC</sub>	EN = V <sub>CC</sub> or V <sub>L</sub>	5	10	20	kΩ
I/O V <sub>CC</sub> Source Current During Low-to-High Transition	I <sub>IHCC</sub>	V <sub>CC</sub> = +1.65V		15		mA
I/O V <sub>CC</sub> Sink Current During High-to-Low Transition	I <sub>ILCC</sub>	V <sub>CC</sub> = +1.65V		10		mA
I/O V <sub>CC</sub> Low-to-High Transition Threshold	V <sub>CC-TH</sub>	V <sub>CC</sub> = +3.3V, V <sub>L</sub> = +1.8V	0.3 x V <sub>CC</sub>	0.5 x V <sub>CC</sub>		V
I/O V <sub>CC</sub> Output-Voltage Low	V <sub>OLC</sub>	I/O V <sub>CC</sub> sink current = 4mA, V <sub>IOVL</sub> = 0V			0.25	V
		I/O V <sub>CC</sub> sink current = 8mA, V <sub>IOVL</sub> ≤ 0.4V or 0.2 x V <sub>L</sub>			V <sub>ILL</sub> + 0.4V	
I/O V <sub>CC</sub> Tri-State Output Leakage Current		EN = GND, T <sub>A</sub> = +25°C	-1		+1	μA
EN Input-Voltage High Threshold	V <sub>IHE</sub>				0.7 x V <sub>L</sub>	V
EN Input-Voltage Low Threshold	V <sub>ILE</sub>		0.3 x V <sub>L</sub>			V
EN Pin Input Leakage Current		T <sub>A</sub> = +25°C	-1		+1	μA
<b>ESD PROTECTION</b>						
I/O V <sub>CC</sub> ESD Protection		C <sub>VCC</sub> = 1μF, Human Body Model		±15		kV

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## TIMING CHARACTERISTICS

( $V_{CC} = +1.65V$  to  $+5.5V$ ,  $V_L = +1.2V$  to  $V_{CC}$ ;  $C_{IOVL} \leq 15pF$ ,  $C_{IOVCC} \leq 15pF$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC}$ _ Rise Time	$t_{RVCC}$	Push-pull driver, Figure 1			50	ns
		Open-drain driver, internal pullup, Figure 2			500	
I/O $V_{CC}$ _ Fall Time	$t_{FVCC}$	Push-pull driver, Figure 1			50	ns
		Open-drain driver, internal pullup, Figure 2			50	
I/O $V_L$ _ Rise Time	$t_{RVL}$	Push-pull driver, Figure 3			50	ns
		Open-drain driver, internal pullup, Figure 4			500	
I/O $V_L$ _ Fall Time	$t_{FVL}$	Push-pull driver, Figure 3			50	ns
		Open-drain driver, internal pullup, Figure 4			50	
Propagation Delay	$t_{I/OVL-VCC}$	Push-pull driver, Figure 1			50	ns
		Open-drain driver, internal pullup, Figure 2			600	
	$t_{I/OVCC-VL}$	Push-pull driver, Figure 3			50	
		Open-drain driver, internal pullup, Figure 4			600	
Propagation Delay After EN	$t_{EN}$	Push-pull or open-drain driver, Figure 5			5	$\mu s$
Channel-to-Channel Skew	$t_{SKEW}$	Push-pull driver			5	ns
		Open-drain driver, internal pullup			100	
Maximum Data Rate		Push-pull driver, Figures 1, 3			6	Mbps
		Open-drain driver, internal pullup, Figures 2, 4			1	

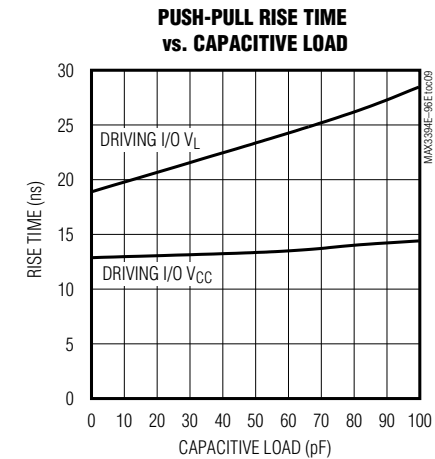
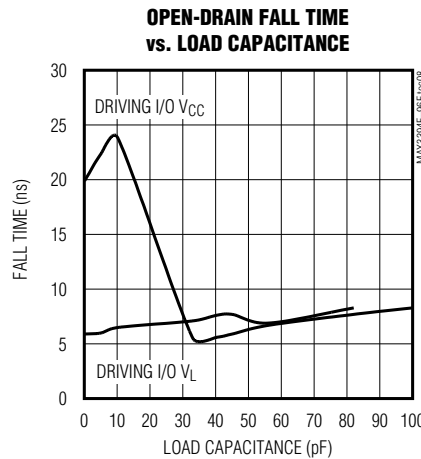
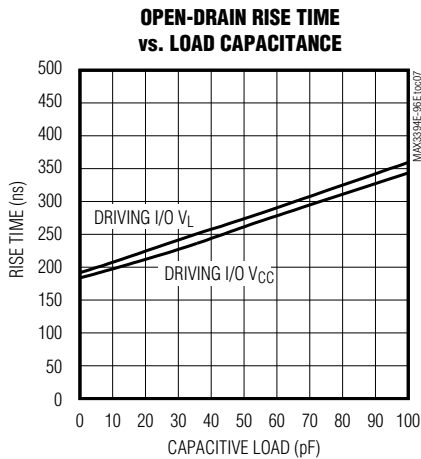
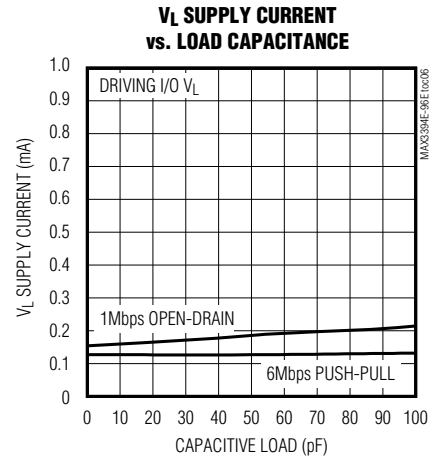
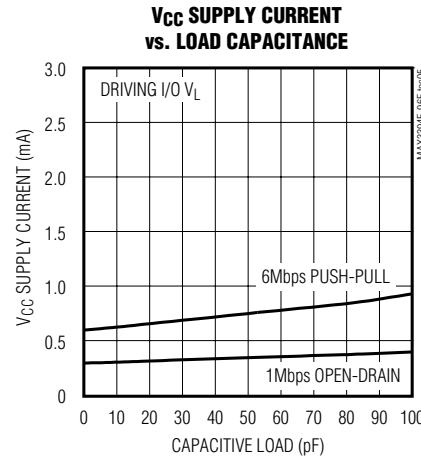
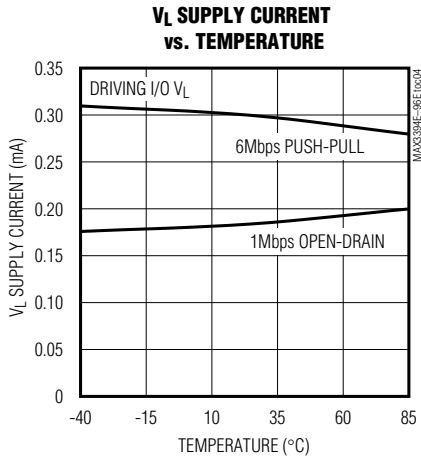
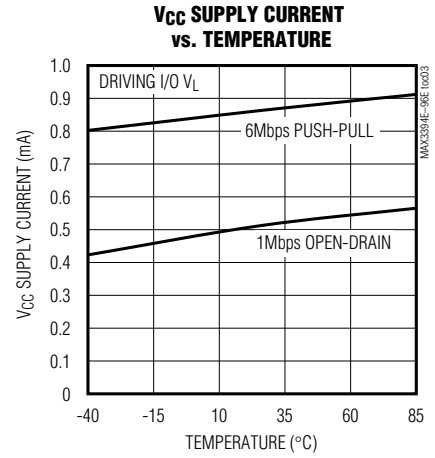
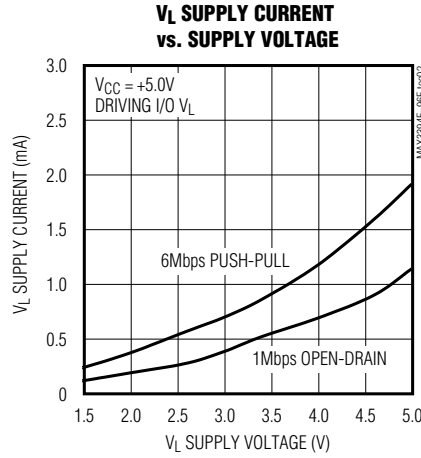
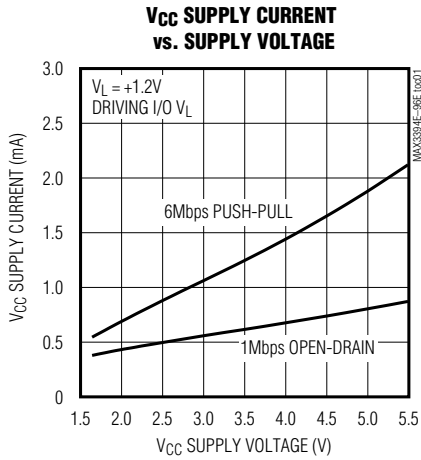
**Note 1:** All units are 100% production tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range are guaranteed by design and not production tested.

**Note 2:** During a low-to-high transition, the threshold at which the I/O changes state is the lower of  $V_{ILL}$  and  $V_{ILC}$  since the two sides are internally connected by an internal switch while the device is in the logic-low state.

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Typical Operating Characteristics

( $V_{CC} = +2.5V$ ,  $V_L = +1.8V$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

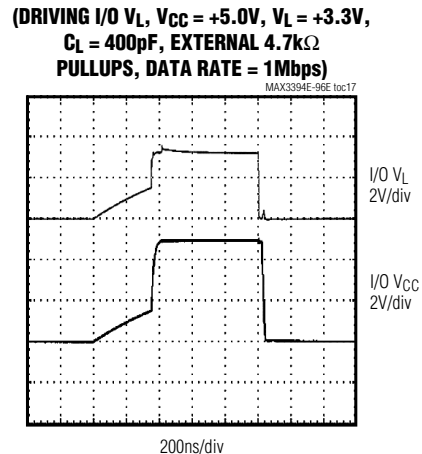
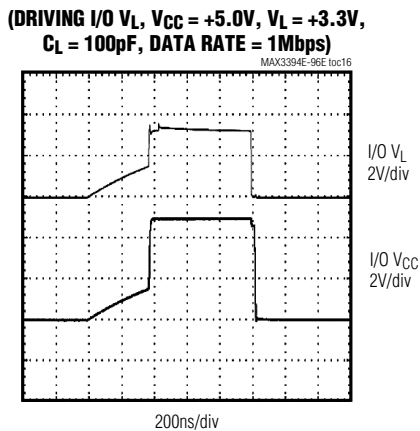
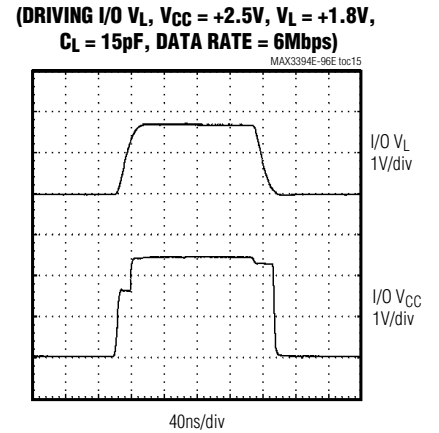
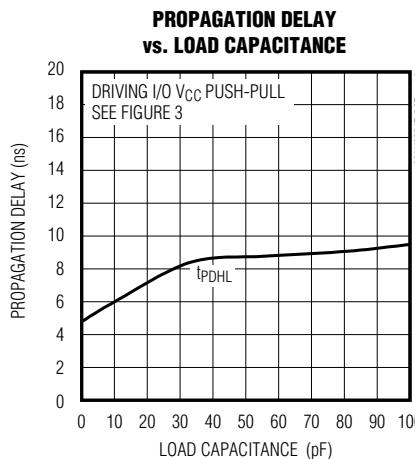
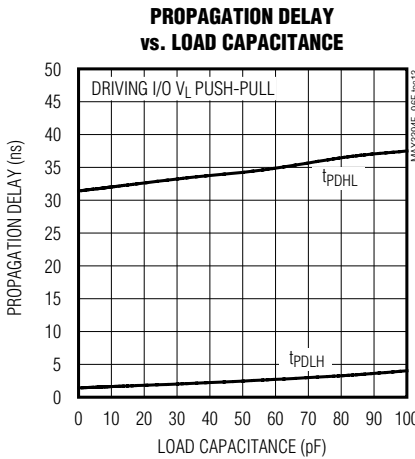
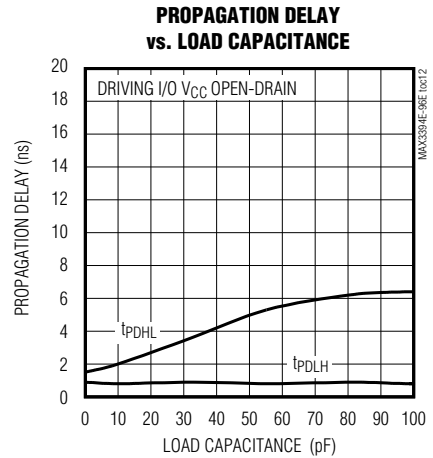
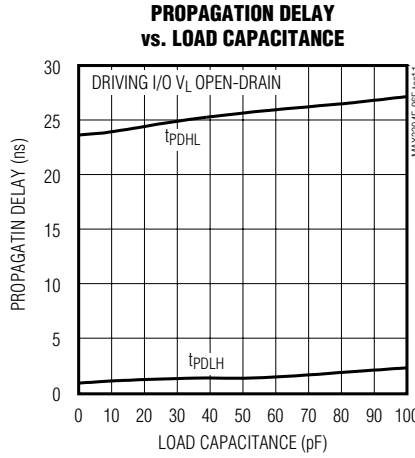
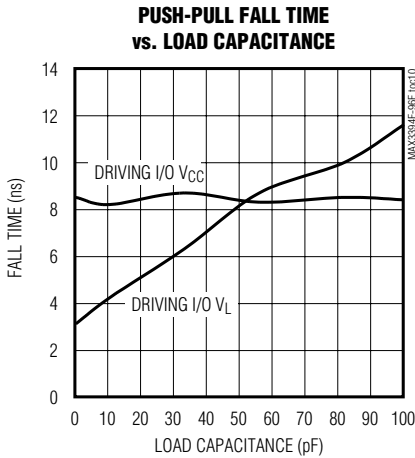


MAX3394E/MAX3395E/MAX3396E

# **$\pm 15kV$ ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry**

## **Typical Operating Characteristics (continued)**

( $V_{CC} = +2.5V$ ,  $V_L = +1.8V$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Pin Description

MAX3394E/MAX3395E/MAX3396E

PIN						NAME	FUNCTION
MAX3394E		MAX3395E		MAX3396E			
TDFN	UCSP	TQFN	UCSP	TQFN	UCSP		
1	A1	11	B1	14	D3	V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage +1.65V ≤ V <sub>CC</sub> ≤ +5.5V. Bypass V <sub>CC</sub> to GND with a 0.1μF ceramic capacitor and a 1μF or greater ceramic capacitor as close to the device as possible.
2	B1	6	B3	4	A4	EN	Enable Input. Drive EN logic high for normal operation. Drive EN logic low to force all I/O lines to a high-impedance state and disconnect internal pullup resistors.
3	A2	10	C1	18	C1	I/O V <sub>CC</sub> 1	I/O 1 Referred to V <sub>CC</sub>
4	A3	9	C2	16	D1	I/O V <sub>CC</sub> 2	I/O 2 Referred to V <sub>CC</sub>
5	B3	5	B4	13	D4	GND	Ground
6	C3	2	A2	20	A1	I/O V <sub>L</sub> 2	I/O 2 Referred to V <sub>L</sub>
7	C2	1	A1	19	B1	I/O V <sub>L</sub> 1	I/O 1 Referred to V <sub>L</sub>
8	C1	12	B2	3	A3	V <sub>L</sub>	Logic Supply Voltage +1.2V ≤ V <sub>L</sub> ≤ V <sub>CC</sub> . Bypass V <sub>L</sub> to GND with a 0.1μF or greater ceramic capacitor as close to the device as possible.
—	—	3	A3	1	B2	I/O V <sub>L</sub> 3	I/O 3 Referred to V <sub>L</sub>
—	—	4	A4	2	A2	I/O V <sub>L</sub> 4	I/O 4 Referred to V <sub>L</sub>
—	—	7	C4	15	D2	I/O V <sub>CC</sub> 4	I/O 4 Referred to V <sub>CC</sub>
—	—	8	C3	17	C2	I/O V <sub>CC</sub> 3	I/O 3 Referred to V <sub>CC</sub>
—	—	—	—	12	C3	I/O V <sub>CC</sub> 5	I/O 5 Referred to V <sub>CC</sub>
—	—	—	—	11	D5	I/O V <sub>CC</sub> 6	I/O 6 Referred to V <sub>CC</sub>
—	—	—	—	10	C4	I/O V <sub>CC</sub> 7	I/O 7 Referred to V <sub>CC</sub>
—	—	—	—	9	C5	I/O V <sub>CC</sub> 8	I/O 8 Referred to V <sub>CC</sub>
—	—	—	—	5	B3	I/O V <sub>L</sub> 5	I/O 5 Referred to V <sub>L</sub>
—	—	—	—	6	A5	I/O V <sub>L</sub> 6	I/O 6 Referred to V <sub>L</sub>
—	—	—	—	7	B4	I/O V <sub>L</sub> 7	I/O 7 Referred to V <sub>L</sub>
—	—	—	—	8	B5	I/O V <sub>L</sub> 8	I/O 8 Referred to V <sub>L</sub>
EP	—	EP	—	EP	—	EP	Exposed Pad. Connect exposed pad to GND.

### Detailed Description

The MAX3394E/MAX3395E/MAX3396E bidirectional level translators provide level shifting required for data transfer in a multivoltage system. Internal slew-rate enhancement circuitry features 10mA current-sink and 15mA current-source drivers to isolate capacitive loads from lower current drivers. In open-drain systems, slew-rate enhancement enables fast data rates with larger

pullup resistors and increased bus load capacitance. Externally applied voltages, V<sub>CC</sub> and V<sub>L</sub>, set the logic-high levels for the device. A logic-low signal on one I/O side of the device appears as a logic-low signal on the opposite I/O side and vice-versa. Each I/O line is pulled up to V<sub>CC</sub> or V<sub>L</sub> by an internal pullup resistor, allowing the devices to be driven by either push-pull or open-drain drivers.

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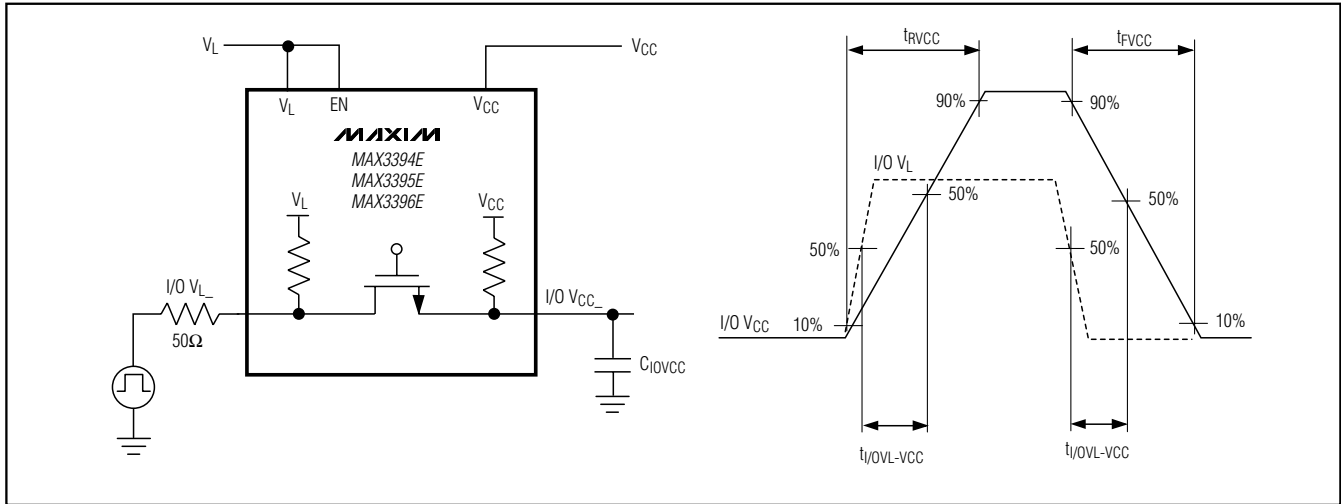


Figure 1. Push-Pull Driving I/O  $V_{L\_}$  Test Circuit and Timing

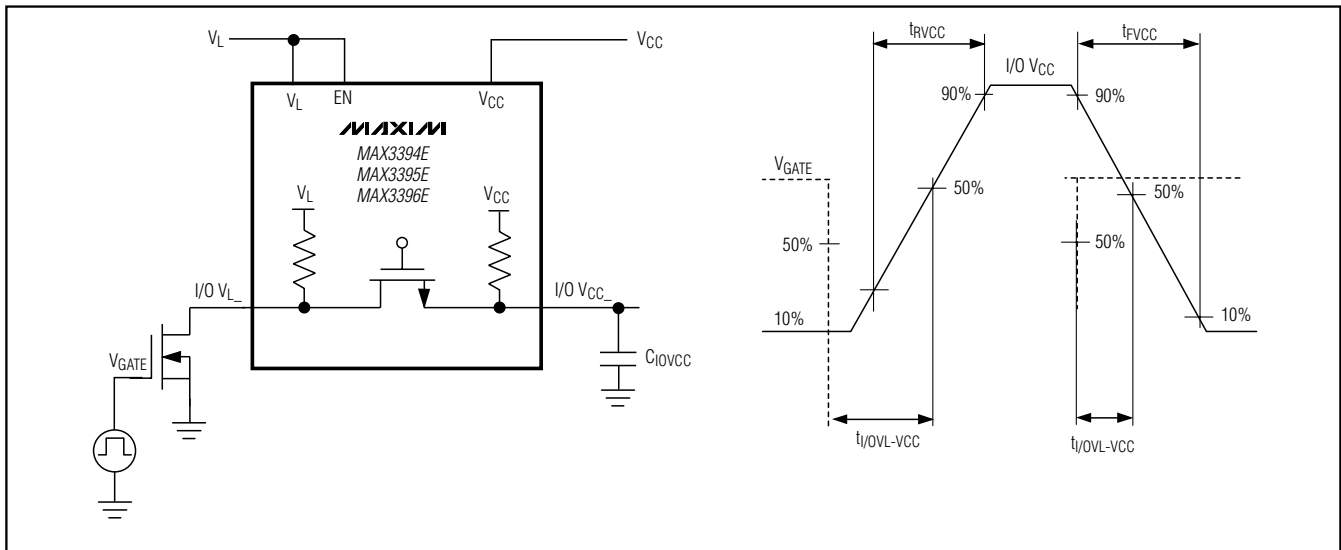


Figure 2. Open-Drain Driving I/O  $V_{L\_}$  Test Circuit and Timing

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The MAX3394E/MAX3395E/MAX3396E accept  $V_{CC}$  voltages from +1.65V to +5.5V, and  $V_L$  voltages from +1.2V to  $V_{CC}$ , making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX3394E/MAX3395E/MAX3396E operate at a guaran-

teed data rate of 6Mbps with push-pull drivers and 1Mbps with open-drain drivers.

### Level Translation

The MAX3394E/MAX3395E/MAX3396E utilize a transmission gate architecture to provide bidirectional level translation between I/O  $V_{L\_}$  and I/O  $V_{CC\_}$ . The transmission gate architecture is comprised of a pass-FET, gate-control logic, and slew-rate enhancement circuitry. When both I/O  $V_{L\_}$  and I/O  $V_{CC\_}$  are logic high, the gate-control logic disables the pass-FET, providing



# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

MAX3394E/MAX3395E/MAX3396E

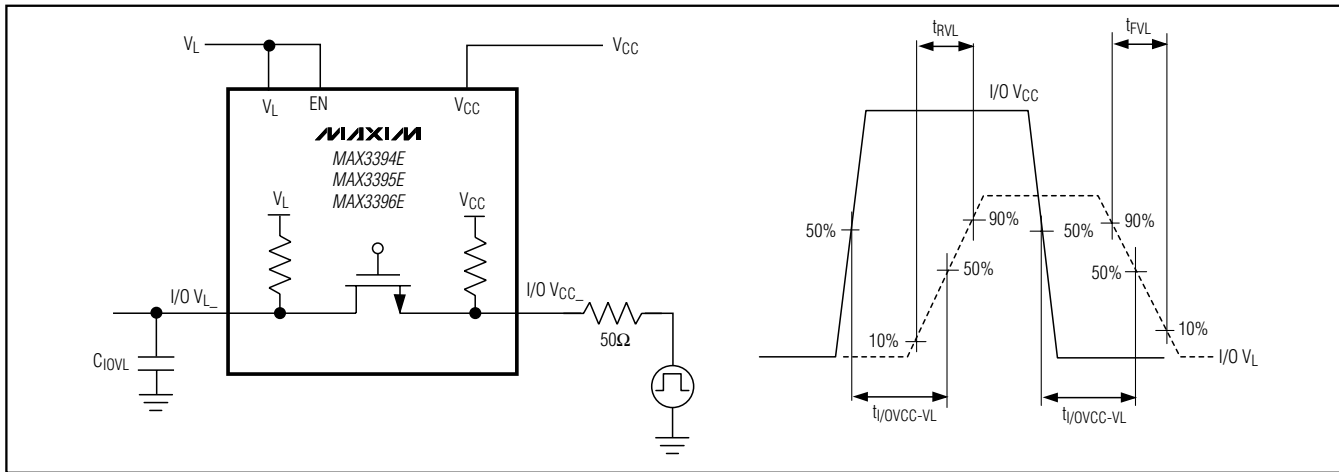


Figure 3. Push-Pull Driving I/O VCC\_ Test Circuit and Timing

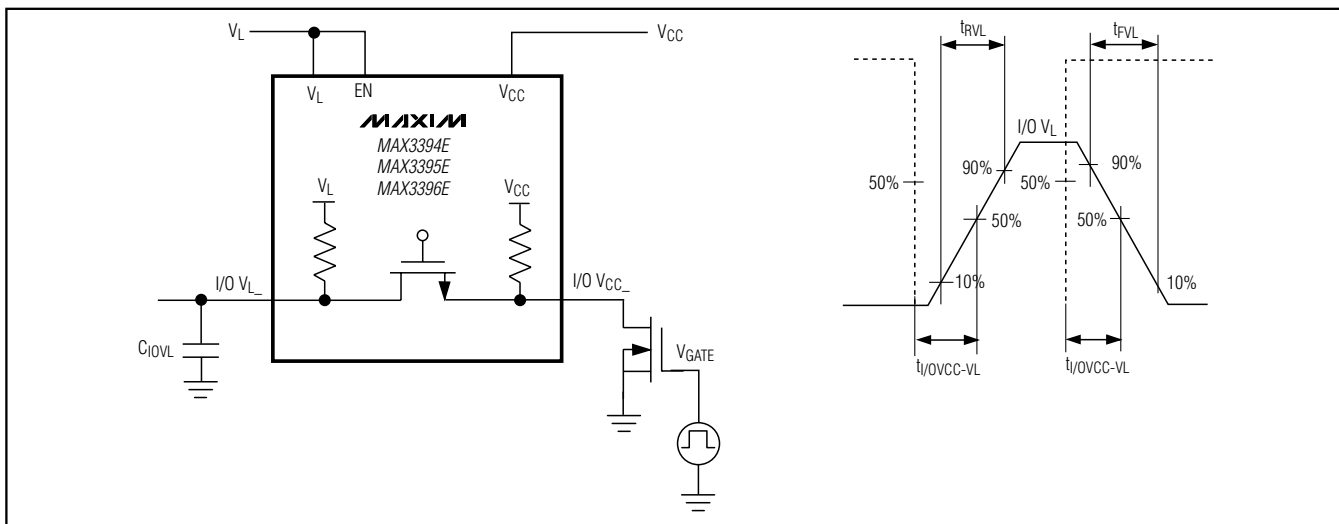


Figure 4. Open-Drain Driving I/O VCC\_ Test Circuit and Timing

capacitive isolation between I/O lines. When one or both I/O lines are at a logic-low level, the gate-control logic turns the pass-FET on. When the pass-FET is active, I/O V\_L\_ and I/O V\_CC\_ are connected, allowing the logic-low signal to be expressed simultaneously on both I/O lines.

The MAX3394E/MAX3395E/MAX3396E have internal 10kΩ (typ) pullup resistors from I/O V\_L\_ and I/O V\_CC\_ to the respective supply voltages, allowing operation with open-drain drivers. Internal slew-rate enhancement circuitry accelerates logic-state transitions, maintaining a fast data rate with a higher bus load capacitance. Additionally, the 10mA current sink drivers permit the use of smaller external pullup resistors.

### Internal Slew-Rate Enhancement

Internal slew-rate enhancement circuitry accelerates logic-state changes by turning on MOSFETs MP<sub>1</sub> and MP<sub>2</sub> during low-to-high logic transitions, and MOSFETs MN<sub>3</sub> and MN<sub>4</sub> during high-to-low logic transitions (see the *Functional Diagram*). During logic-state changes, speed-up MOSFETs are triggered by I/O line voltage thresholds. MOSFETs MN<sub>3</sub> and MN<sub>4</sub> sink 10mA during high-to-low logic transitions. MP<sub>1</sub> and MP<sub>2</sub> source 15mA during low-to-high logic transitions. Slew-rate enhancement allows a fast data rate despite large capacitive bus loads, and permits larger external pullup resistors.

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

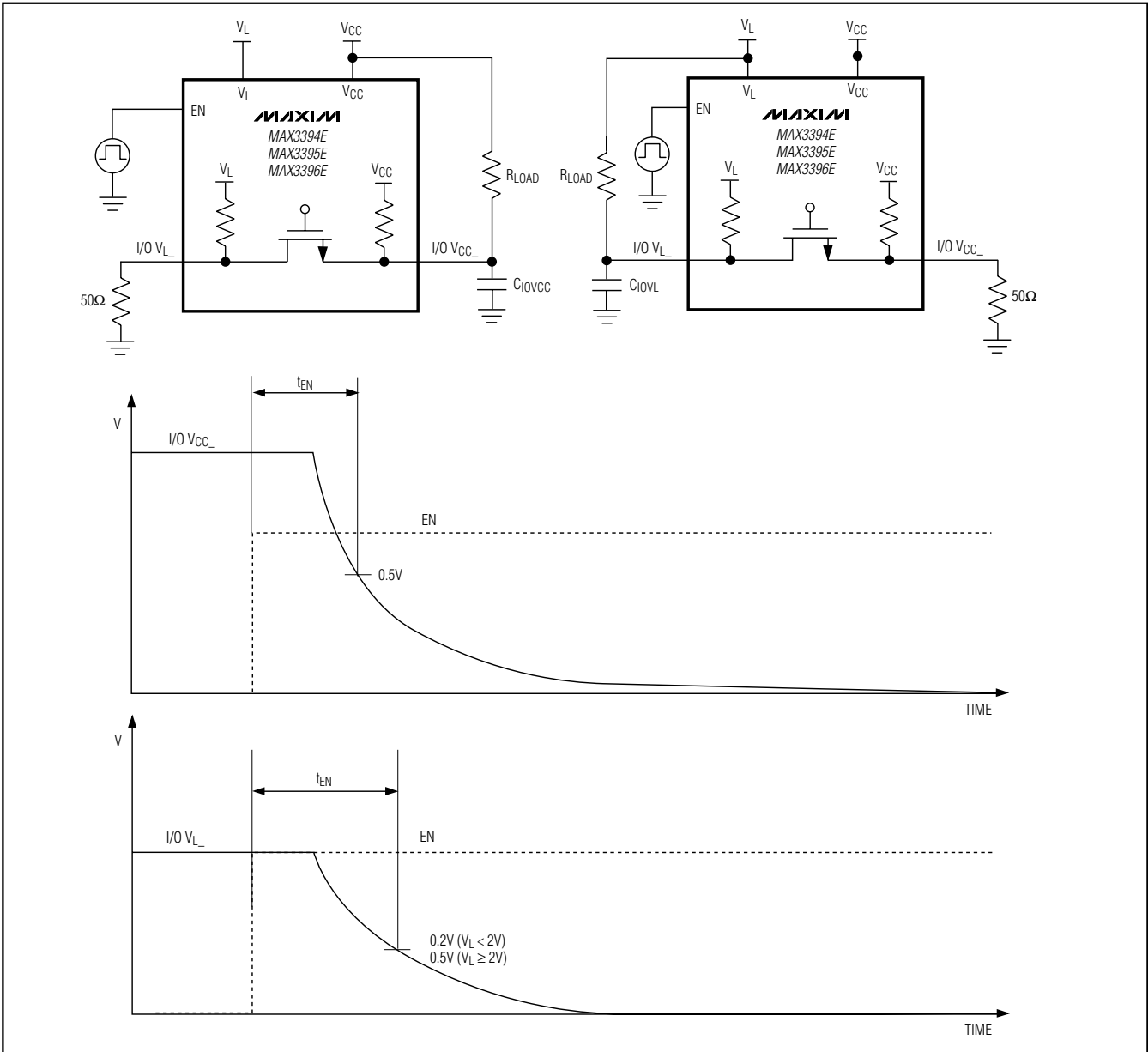


Figure 5. Enable Test Circuit and Timing

### Power-Supply Sequencing

The MAX3394E/MAX3395E/MAX3396E require two supply voltages. For proper operation, ensure that  $+1.65V \leq V_{CC} \leq +5.5V$ , and  $+1.2V \leq V_L \leq V_{CC}$ . There are no restrictions on power-supply sequencing. During power-up or power-down, the MAX3394E/MAX3395E/MAX3396E can withstand either the  $V_L$  or the  $V_{CC}$  supply floating while the other supply is applied. The device will not latch up in this state.

### Tri-State Output Mode

Connect EN to  $V_L$  or  $V_{CC}$  for normal operation. Drive EN low to force the MAX3394E/MAX3395E/MAX3396E to a tri-state output mode. In tri-state output mode, all I/O lines are driven to a high-impedance state, and the pass-FET is disabled to prevent current flow between I/O lines. Tri-state output mode disables the internal pullup resistors on I/O  $V_L$  and I/O  $V_{CC}$ , and reduces supply current to  $3\mu A$  typ ( $V_{CC}$ ) and  $0.7\mu A$  typ ( $V_L$ ).

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

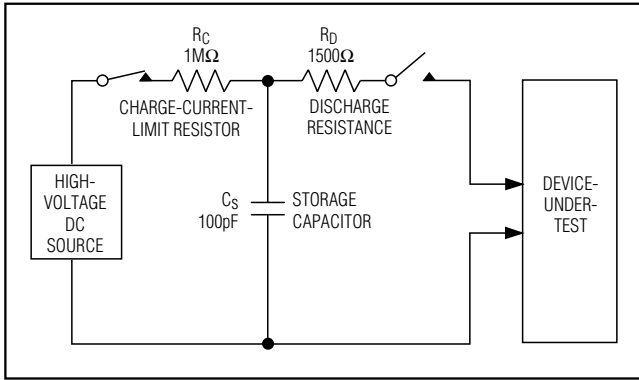


Figure 6a. Human Body ESD Test Model

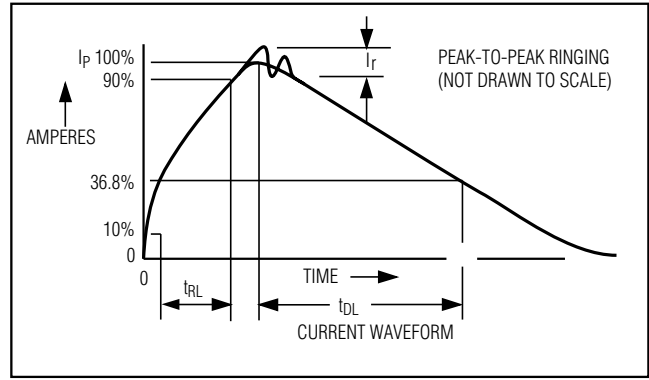


Figure 6b. HBM Discharge Current Waveform

The high-impedance state of the I/O lines during tri-state output mode facilitates use in multidrop networks. In tri-state output mode, do not exceed  $(V_L + 0.3V)$  on I/O  $V_L$  or  $(V_{CC} + 0.3V)$  on I/O  $V_{CC}$ .

### Thermal-Shutdown Protection

The MAX3394E/MAX3395E/MAX3396E are protected from thermal damage resulting from short-circuit faults. In the event of a short-circuit fault, when the junction temperature ( $T_J$ ) reaches  $+125^\circ\text{C}$ , a thermal sensor forces the device into the tri-state output mode. When  $T_J$  drops below  $+115^\circ\text{C}$ , normal operation resumes.

### ±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The I/O  $V_{CC}$  lines are further protected by advanced ESD structures to guard these pins from damage caused by ESD of up to  $\pm 15\text{kV}$ . Protection structures prevent damage caused by ESD events in normal operation, tri-state output mode, and when the device is unpowered. After arresting an ESD event, MAX3394E/MAX3395E/MAX3396E continue to function without latching up, whereas competing devices can enter a latched-up state and must be power cycled to restore functionality.

Several ESD testing standards exist for gauging the robustness of ESD structures. The ESD protection of the MAX3394E/MAX3395E/MAX3396E is characterized for the human body model (HBM). Figure 6a shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage then discharged through a 1.5kΩ resistor. Figure 6b shows the current waveform when the storage capacitor is discharged into a low impedance.

To ensure full  $\pm 15\text{kV}$  ESD protection, bypass  $V_{CC}$  to ground with a 0.1μF ceramic capacitor and an additional 1μF ceramic capacitor as close to the device as possible.

### ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report documenting test setup, methodology, and results.

## Applications Information

### Power-Supply Decoupling

Bypass  $V_L$  and  $V_{CC}$  to ground with 0.1μF ceramic capacitors. To ensure full  $\pm 15\text{kV}$  ESD protection, bypass  $V_{CC}$  to ground with an additional 1μF or greater ceramic capacitor. Place all capacitors as close to the device as possible.

### Open-Drain Mode vs. Push-Pull Mode

The MAX3394E/MAX3395E/MAX3396E are compatible with push-pull (active) and open-drain drivers. For push-pull operation, maximum data rate is guaranteed to 6Mbps. For open-drain applications, the MAX3394E/MAX3395E/MAX3396E include internal pullup resistors and slew-rate enhancement circuitry, providing a maximum data rate of 1Mbps. External pullup resistors can be added to increase data rate when the bus is loaded by high capacitance. (See the *Use of External Pullup Resistors* section.)

### Serial-Interface Level Translation

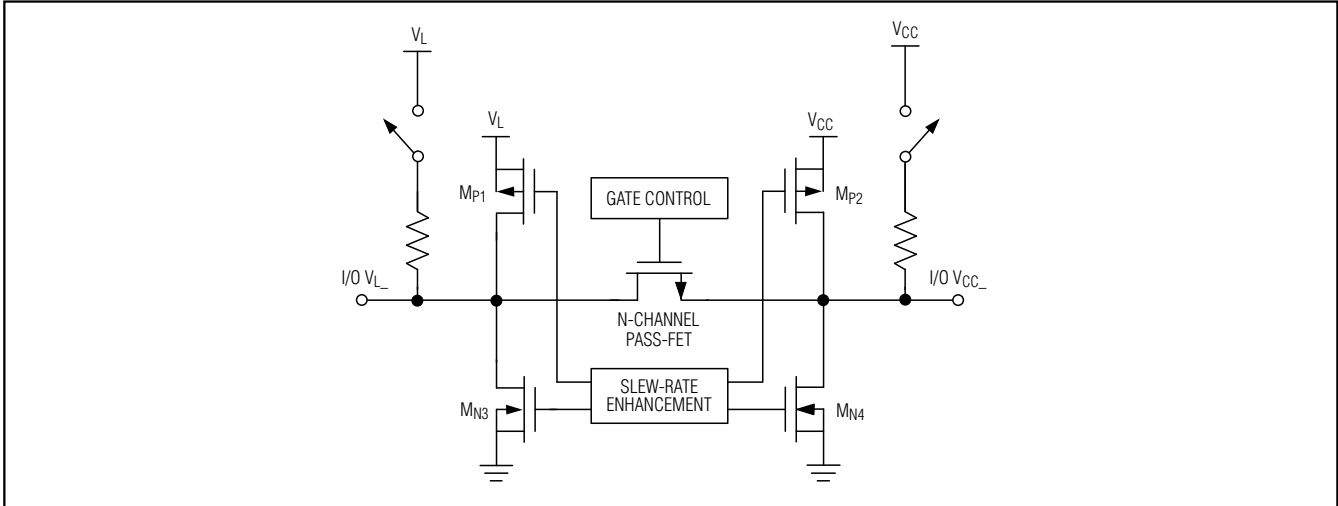
The MAX3395E provides level translation on four I/O lines, making it an ideal device for multivoltage I<sup>2</sup>C, MICROWIRE, and SPI serial interfaces.

### Use of External Pullup Resistors

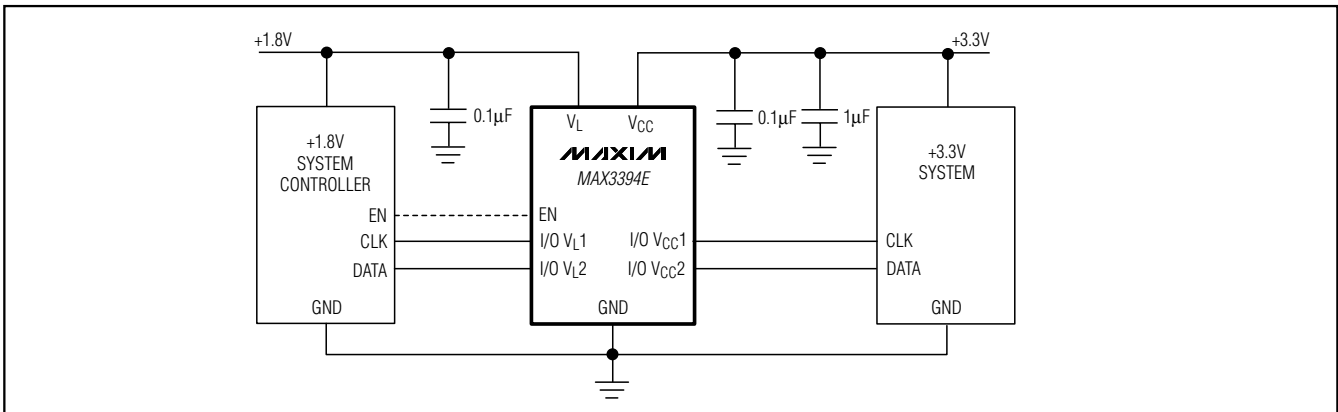
The MAX3394E/MAX3395E/MAX3396E include internal 10kΩ pullup resistors. During a low-to-high logic transition, the internal pullup resistors charge the bus capacitance with a characteristic RC charging waveform.

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Functional Diagram



## Typical Operating Circuit



When the low-to-high transition threshold ( $V_{CC-TH}$  or  $V_{L-TH}$ ) is reached, the rise time accelerators switch on, sourcing 15mA to fully charge the bus capacitance. External pullup resistors reduce the time needed to reach the low-to-high transition threshold, thereby increasing the data rate. In the logic-low state however, external pullup resistors increase the DC current through the internal pass-FET, increasing the output voltage of the device.

### Smart-Card Interface

The MAX3395E provides level translation for Class A, B, and C smart cards. When supply voltage  $V_{CC}$  is interrupted due to the disconnection of a smart card, the device does not latch up. Normal operation resumes upon restoration of the  $V_{CC}$  supply voltage. The

MAX3395E provides bidirectional level translation on four I/O lines, making it well suited for buffering and translating 4-wire serial interfaces.

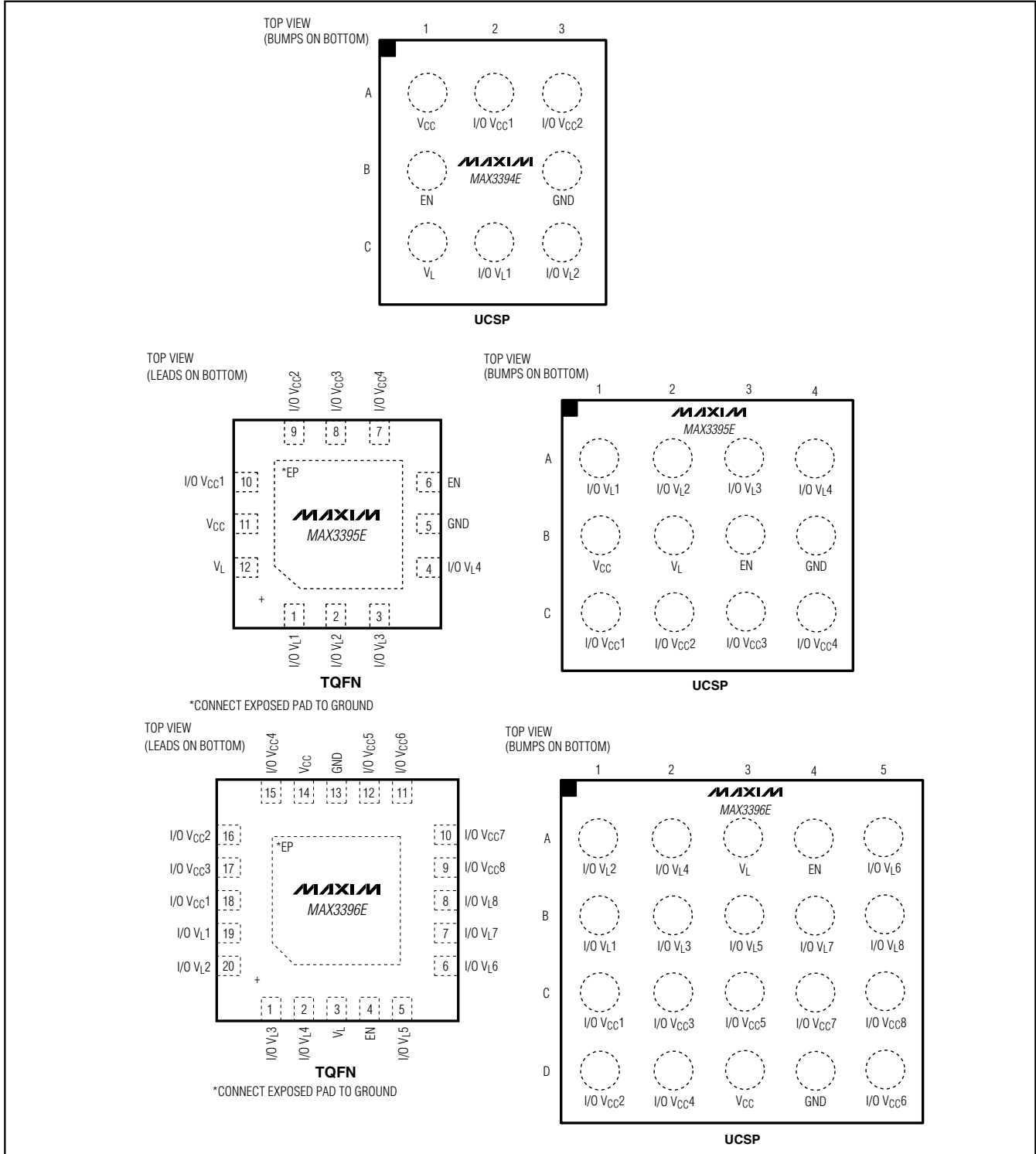
### UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profiles, as well as the latest information on reliability testing results, go to Maxim's web site at [www.maxim-ic.com/ucsp](http://www.maxim-ic.com/ucsp) to find the Application Note: *UCSP-A Wafer-Level Chip-Scale Package*.

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Pin Configurations (continued)

**MAX3394E/MAX3395E/MAX3396E**



# **±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry**

## **Selector Guide**

<b>PART</b>	<b>NUMBER OF TRANSLATORS</b>	<b>TOP MARK</b>
MAX3394EETA+T	2	APE
MAX3394EEBL+T	2	AEZ
MAX3395EETC+	4	AAFZ
MAX3395EEBC+T	4	ACO
MAX3396EEBP+T*	8	—
MAX3396EETP+*	8	—

**Note:** All devices specified over the -40°C to +85°C operating range.

\*Future product—contact factory for availability.

+Denotes lead-free package.

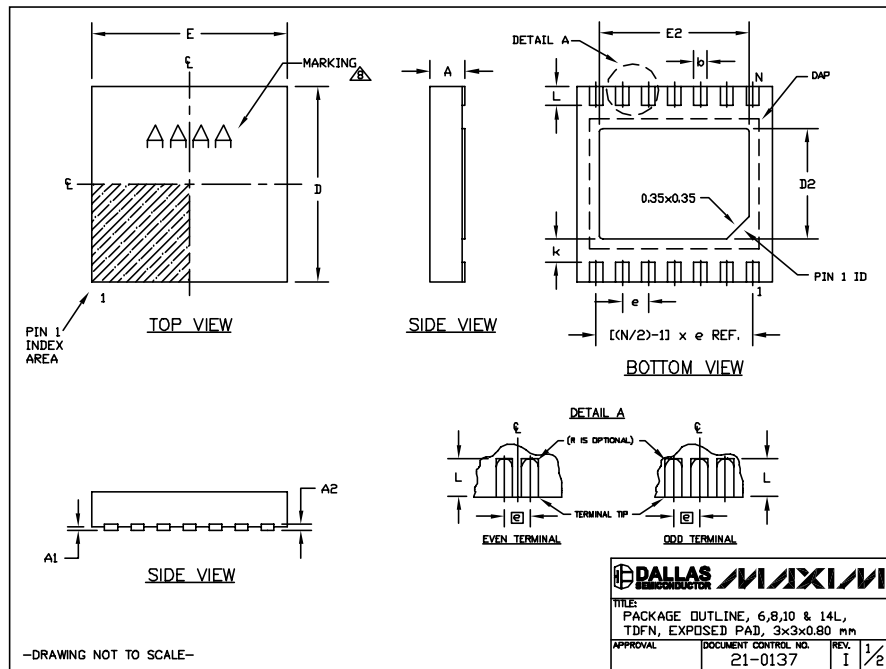
## **Chip Information**

PROCESS: BiCMOS

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



6, 8, & 10L, DFN THINLEPS

COMMON DIMENSIONS			PACKAGE VARIATIONS							
SYMBOL	MIN.	MAX.	PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
A	0.70	0.80	T833-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
D	2.90	3.10	T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
E	2.90	3.10	T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
A1	0.00	0.05	T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
L	0.20	0.40	T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
k	0.25 MIN.		T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
A2	0.20 REF.		T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF

NOTES:  
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.  
 2. COPLANARITY SHALL NOT EXCEED 0.08 mm.  
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.  
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).  
 5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.  
 6. "N" IS THE TOTAL NUMBER OF LEADS.  
 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.  
 MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

APPROVAL	DOCUMENT CONTROL NO.	REV.	2/2
	21-0137	I	

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**TOP VIEW**

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2

**NOTES:**  
 1. ALL DIMENSIONS ARE IN MILLIMETERS.  
 2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

**BOTTOM VIEW**

**SIDE VIEW**

TITLE: PACKAGE OUTLINE, 3x3 UCSP		
APPROVAL	DOCUMENT CONTROL NO. 21-0093	REV. K 1/1

-DRAWING NOT TO SCALE-

9LUCSP, 3x3 EFS



# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX3394E/MAX3395E/MAX3396E

**TOP VIEW**

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3

**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

**BOTTOM VIEW**

**SIDE VIEW**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

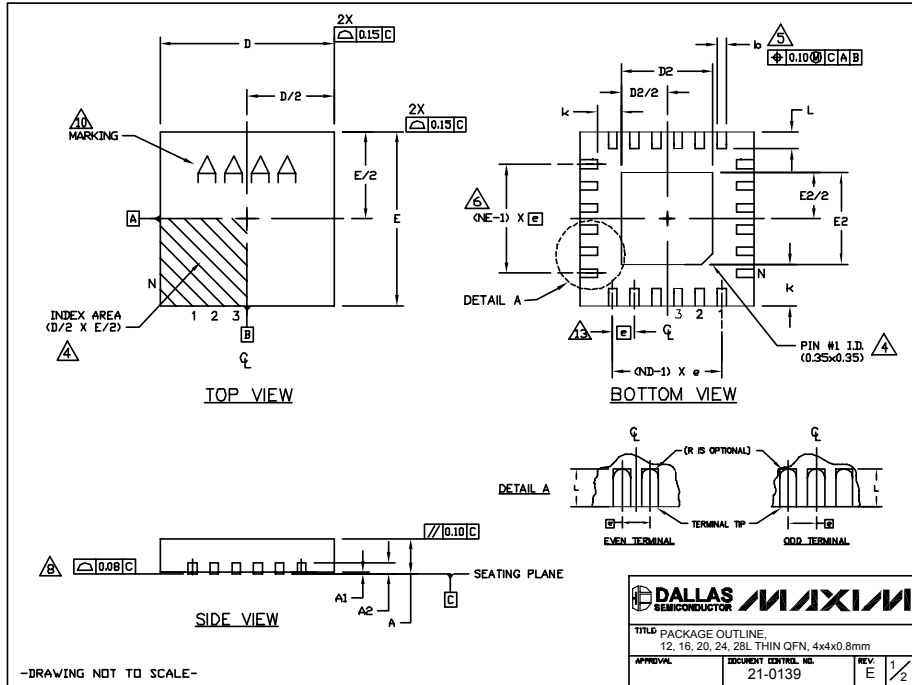
APPROVAL	DOCUMENT CONTROL NO. 21-0104	REV. F	1/1
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12L UCSP 4x3EPS

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



PKG REF.	COMMON DIMENSIONS												EXPOSED PAD VARIATIONS						
	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			DOWN BOND ALLOWED			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.				
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	YES			
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	NO			
A2	0.20	REF.		0.20	REF.		0.20	REF.		0.20	REF.		0.20	REF.		YES			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	NO			
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	YES			
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	NO			
e	0.80	BSC.		0.65	BSC.		0.50	BSC.		0.50	BSC.		0.40	BSC.		YES			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	YES			
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	NO			
N	12			16			20			24			28			NO			
ND	3			4			5			6			7			NO			
NE	3			4			5			6			7			NO			
Package Code	VGG3			VGGC			WGGD-1			WGGD-2			VGGE						

**NOTES:**

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC M0220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- COPLANARITY SHALL NOT EXCEED 0.08mm
- WARPAGE SHALL NOT EXCEED 0.10mm
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "c", ±0.05.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

**DALLAS SEMICONDUCTOR MAXIM**  
 TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN OFN, 4x4x0.8mm  
 APPROVAL: DOCUMENT CONTROL NO. 21-0139 REV. E 2/2

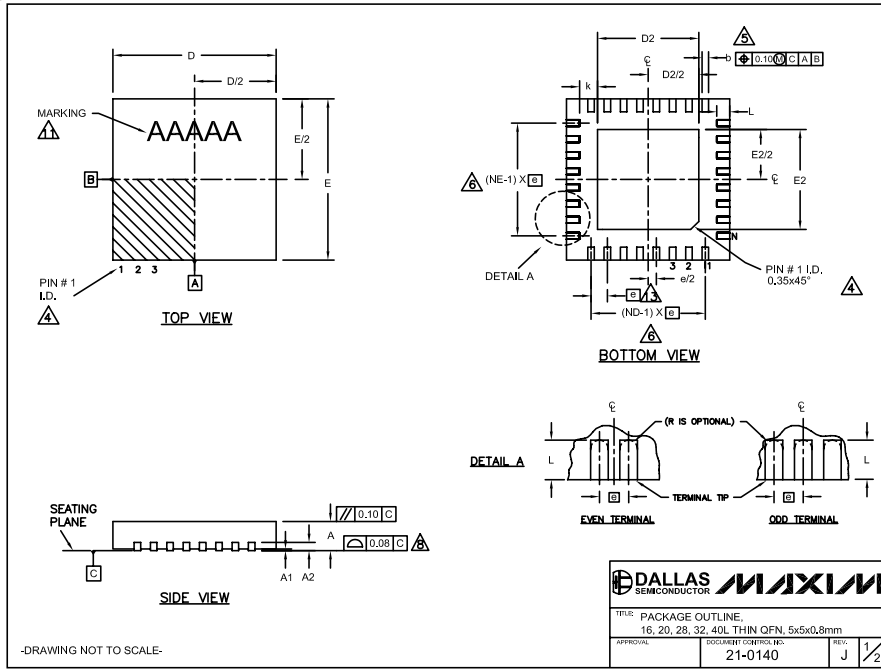
-DRAWING NOT TO SCALE-

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX3394E/MAX3395E/MAX3396E



COMMON DIMENSIONS															
PKG. SYMBOL	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			---		

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

\*\*SEE COMMON DIMENSIONS TABLE

-DRAWING NOT TO SCALE-

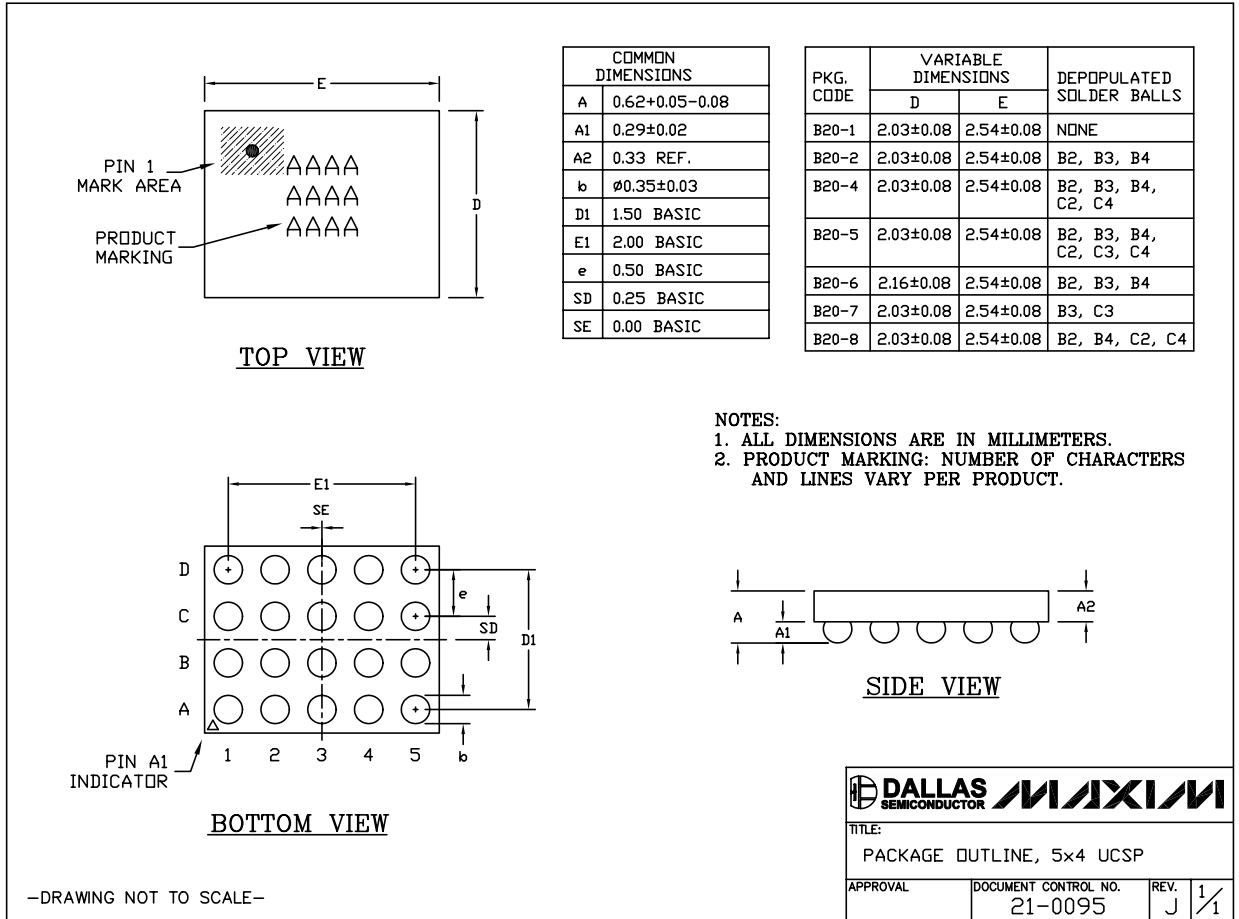
<b>DALLAS SEMICONDUCTOR</b>		<b>MAXIM</b>	
TITLE: PACKAGE OUTLINE			
16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	J 2/2
21-0140			

- NOTES:
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
  - ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
  - N IS THE TOTAL NUMBER OF TERMINALS.
  - THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
  - DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
  - ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
  - DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
  - COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
  - DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
  - WARPAGE SHALL NOT EXCEED 0.10 mm.
  - MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
  - NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
  - LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

# ±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



5x4 UCSP.EPS

## Revision History

Pages changed at Rev 2: 1-4, 9, 11, 12, 14, 20

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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